**M.S. Ramaiah Institute of Technology**

**(Autonomous Institute, Affiliated to VTU)**

**Department of CSE**

**CIE II- Scheme and Solutions**

**Course:** Computer Organization **Course Code:** CS1541  **Sem:** IV **Max Marks:** 30

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sl#** | | **Part A**  **(Answer All the questions)** | **Marks** | **Bloom’s Level** |
| 1 | | 5\*1=5M   1. -52 is stored in 32-bit memory as 1111 1111…001100(32 bits) 2. Compare B and BL instructions   B is for simple branch and BL(branch and link) is used to call procedure   1. List out all the hardware design principles. (2M)  * Simplicity favors regularity * Smaller is faster * Common case is made faster * Good design comes along with good compromise  1. State True/False   i) r9 register is preserved on procedure call: True  ii)Process of putting more commonly used variables into memory is called spilling register: False. | 5 | Remember |
| **Sl#** | **Part B**  **(Answer All the Questions)** |  |  |
| 2 | Program carries 5M  Mov r1, #0  Mov r2, #0  Bl leaf  Leaf: sub sp,sp, #4  Str r4, [sp, #0]  L1: ldrb r4, [r0,r2]  Add r1, r1, #1  Cmp r4, #0  Add sp, sp #4  Mov pc,lr  Add r2, r2, #1  B L1  Add sp, sp #4  Mov pc, lr | 5 | Apply |
| 3 | i) STR r2, [r6, #40] 1.5M   |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | 14 | 1 | 25 | 6 | 2 | 40 |   ii)ADD r7, r2, r6 ,LSL r4 2M   |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 14 | 0 | 0 | 4 | 0 | 2 | 7 | 4 0 | 0 | 1 | 6 |   General instruction format 1.5M   |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | | cond | F | I | opcode | s | Rn | Rd | Rs/operand | | 5 | Apply |
| 4 | Scaled register offset pre-indexed addressing mode.  Explanation 3M diagram 2M  [Rn, ±Rm, shift]!  Scaled register pre-indexed Address accessed is as with scaled register offset mode, but Rn's value updates to become the address accessed.  e.g  ldr r2, [r0, r1, lsl #2]!  r0 ← r0 + r1\*4  then r2 ← \*r0 | 5 | Understand |
| 5 | Diagram 2M Explanation 3M | 5 | Understand |
| 6 | 1. Perform 78 x - 42 using Booth algorithm 2M   M=1001110  Q=1010110  2’s complement of m=0110010  Recoding of Q 10101100=-1+1 -1 +1 0 -1 0  1001110  -1 1 -1 1 0 -1 0  1111110110010X  00001001110XXX  1110110010XXXX  001001110XXXXX  10110010XXXXXX  11001100110100  b)52 x 32 using sequential multiplier circuit 3M   |  |  |  |  | | --- | --- | --- | --- | | Operation | C | A | Q | |  | 0 | 000000 | 100011 | | Add+Shift | 0 | 011111 | 010001 | | Add+Shift | 0 | 101110 | 101000 | | Shift | 0 | 010111 | 010100 | | Shift | 0 | 001011 | 101010 | | Shift | 0 | 000101 | 110101 | | Add+Shift | 0 | 100001 | 111010 | | 5 | Apply |